IR-2257 (2-3684)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of	New York, New York
Martin Standing	Date: May 25, 2005
Serial No.: 10/677,069	Group Art Unit: 2814
Filed: October 1, 2003	Examiner: Nathan W. Ha

For: SEMICONDUCTOR DEVICE PACKAGE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. §1.192

Sir:

This appeal is from the Examiner's final rejection of this application dated November 30, 2004.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is:

International Rectifier Corporation

II. RELATED APPEALS AND INTERFERENCES

The applicant(s), the assignee(s) and the undersigned attorneys are not aware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-5, 7-14, 16-22 are pending and on appeal herein.

Claims 23-27 are withdrawn and not under consideration.

Claims 6 and 15 have been previously canceled.

IV. STATUS OF AMENDMENTS

An amendment dated September 14, 2004 was submitted and entered.

No other amendments are pending disposition.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed at a semiconductor package.

Referring to Figure 7 of the specification, which illustrates an example of the present invention, a semiconductor package according to the present invention includes a first circuit board 12, a second circuit board 14, and at least one semiconductor die T6 disposed between the two circuit boards 12,14. The semiconductor die T6 includes electrodes ST6, and DT6 which are disposed on opposing surfaces thereof. Semiconductor die T6 further includes electrode GT6 on the same surface as electrode ST6. Electrode ST6 is directly connected electrically and mechanically to a respective conductive pad 18T6 on circuit board 14 with a body of conductive adhesive 33 such as solder, or conductive epoxy, and electrode DT6 is directly connected electrically and mechanically to a respective conductive pad 20T6 on circuit board 12 with a body of conductive adhesive 33 such as solder or conductive epoxy. Also, electrode GT6 is directly connected electrically and mechanically to a respective conductive pad 24T6 on circuit board 14 with a body of conductive adhesive 33 such as solder, or conductive epoxy. See specification at page 8, line 12 - page 9, line 5.

Referring to Figure 2, at least one of the circuit boards (e.g. circuit board 12) includes external connectors 16 for external connection to other components. Each electrical connector is a portion of a conductive track on the circuit board which also includes at least one conductive pad that is electrically connected to an electrode of the semiconductor die.

A package according to the present invention is scalable meaning that it can be expanded to include a plurality of semiconductor die which are interconnected inside the package to form one or a plurality of circuits. For example, a package according to the present invention may include a plurality of power switching die for forming half-bridges or converter circuits, as explained in detail throughout the specification.

Thus, claim 1 calls for the following combination:

1. A semiconductor package comprising:

a first circuit board including at least one conductive pad disposed on a major surface thereof;

a second circuit board including at least one conductive pad on a major surface thereof; and

a semiconductor die including a first electrical contact on a first major surface thereof and a second electrical contact on a second major surface thereof;

a first layer of conductive adhesive interposed between, and mechanically connected to, said first electrical contact and said at least one conductive pad on said first circuit board; and

a second layer of conductive adhesive interposed between, and mechanically connected to, said second electrical contact and said at least one conductive pad on said second circuit board; whereby said first electrical contact is electrically connected to said at least one conductive pad on said first circuit board and said second electrical contact is electrically connected to said at least one conductive pad on said second circuit board.

Claim 11 calls for the following combination:

11. A semiconductor package comprising:

a first thermally conductive substrate including a plurality of conductive pads disposed on a first major surface thereof;

a second thermally conductive substrate including a plurality of conductive pads disposed on a first major surface thereof;

a plurality of power semiconductor devices each including a first power contact on a first major surface thereof, a second power contact and a control contact on a second opposing major surface thereof;

a first layer of conductive adhesive interposed between, and mechanically connected to, a first power contact of each power semiconductor device and a respective conductive pad on said first thermally conductive substrate,

a second layer of conductive adhesive interposed between, and mechanically connected to, a second power contact of each power semiconductor device and a respective conductive pad on said second thermally conductive substrate;

and a third layer of conductive adhesive interposed between, and mechanically connected to, a control contact of each power semiconductor device and a respective conductive pad on said second thermally conductive substrate;

whereby each one of said contacts of said power semiconductor devices is electrically connected to a respective one of said plurality of conductive pads, and wherein said conductive pads on said thermally conductive substrate are interconnected to form part of a circuit.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1 and 11 are anticipated under 35 U.S.C. § 102(b) in view of Potter et al., U.S. Patent No. 5,426,263 (the '263 patent).

VII. ARGUMENT

With respect to claim 1 and claim 11 the Examiner has asserted the following:

In regard to claims 1 and 11, in fig. 3, Potter discloses a semiconductor package comprising:

a first circuit board 30 including at least one conductive pad 34 disposed on a major surface thereof;

a second circuit board 32 including at least one conductive pad on a major surface thereof;

a semiconductor die 10 including a first electrical contact, or pad under the member, not shown, on a first major surface thereof and a second electrical contact 18 on a second major surface thereof, not shown;

a first layer of conductive adhesive 18 interposed between, and mechanically connected to the first contact and the at least one conductive pad on the board; and

a second layer of conductive adhesive, also 18, interposed between, and mechanically connected to the electrical contact and the at least one conductive pad 36 on the second circuit board; whereby the first electrical contact is electrically connected to said at least one conductive pad on said first circuit board and said second electrical contact is electrically connected to said at least one conductive pad on said second circuit board.

Component 10 shown by the '263 patent is a leadless package. See specification, Col. 2, lines 30-39. Referring specifically to Figs. 1, and 2a-2d, component 10 includes an integrated circuit chip (IC) 20, which is mounted on a circuit carrying substrate 22. An enclosure 24 encapsulates at least IC 20. The '263 patent states that the "electrical I/Os of the IC 20 are then fed to the package exterior in any number of ways to form electrical terminations 18 on the to 14 and bottom of the package." Col. 2, lines 49-52.

The '263 patent does not specify and its figures do not clearly show a direct connection with solder or the like between the IC 20 pads and a circuit board on the top and a circuit board on the bottom. Indeed, Figs. 2a and 2c only show one substrate 22 and one IC 20. Fig. 2b shows two ICs 20 residing against one another and each connected to a respective substrate 22. Thus, component 10 cannot constitute the subject matter of claims 1 and 11 which call for a single device between two circuit boards.

Furthermore, Fig. 3 shows component 10 (which is a package not a semiconductor die) residing between two circuit boards 30,32.

However, claim 1 calls for:

a semiconductor die including a first electrical contact on a first major surface thereof and a second electrical contact on a second major surface thereof;

a first layer of conductive adhesive interposed between, and mechanically connected to, said first electrical contact and said at least one conductive pad on said first circuit board; and

a second layer of conductive adhesive interposed between, and mechanically connected to, said second electrical contact and said at least one conductive pad on said

second circuit board; whereby said first electrical contact is electrically connected to said at least one conductive pad on said first circuit board and said second electrical contact is electrically connected to said at least one conductive pad on said second circuit board.

Similar limitations are present at least in claim 11 as well.

IC 20 contained in component 10 of the '263 does not correspond to the semiconductor die of claim 1 in that it is electrically connected to conductive pads of either circuit board 30 or 32 through at least some intermediate structure, such as substrate 22, or the mysterious "any number of ways" called for by the '263 patent.

To be specific, the '263 patent does not show or suggest "a first layer of conductive adhesive interposed between, and mechanically connected to, said first electrical contact and said at least one conductive pad on said first circuit board; and a second layer of conductive adhesive interposed between, and mechanically connected to, said second electrical contact and said at least one conductive pad on said second circuit board" as called for by claim 1 and similarly by claim 11.

It should be noted that because of the intermediate structures, a package proposed by the '263 would inherently exhibit a higher overall resistance. Also, due to the additional packaging such as the mold compound one would expect lower thermal performance from the device shown by the '263 patent.

In addition, it is respectfully suggested that the '263 patent cannot establish an anticipation case in that it does not in fact show a die with electrodes on both surfaces thereof. Indeed, the Examiner has recognized that the '263 does not show pads on the second major surface thereof. However, the Examiner appears to have just assumed the presence of such pads without any evidence to establish the necessary presence of the same. In the absence of such evidence, it cannot be assumed that IC 20 necessarily includes conductive pads on both surfaces, and thus cannot anticipate claims 1 and 11.

For these reasons claims 1 and 11 should not be deemed anticipated by the '263 patent.

VIII. CONCLUSION

Claims 1 and 11 are not anticipated by the '263 patent. The rejection of claims 1 and 11 and claims depending from claims 1 and 11 should be reversed.

If this communication is filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 25, 2005

Kourosh Salehi
Name of applicant, assignee or Registered Representative

Signature

Kourosh Salehi
Date of Signature

Respectfully submitted,

Kourosh Salehi
Registration No.: 43,898
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

KS:gl

CLAIMS APPENDIX

1. A semiconductor package comprising:

a first circuit board including at least one conductive pad disposed on a major surface thereof;

a second circuit board including at least one conductive pad on a major surface thereof; and

a semiconductor die including a first electrical contact on a first major surface thereof and a second electrical contact on a second major surface thereof;

a first layer of conductive adhesive interposed between, and mechanically connected to, said first electrical contact and said at least one conductive pad on said first circuit board; and

a second layer of conductive adhesive interposed between, and mechanically connected to, said second electrical contact and said at least one conductive pad on said second circuit board; whereby said first electrical contact is electrically connected to said at least one conductive pad on said first circuit board and said second electrical contact is electrically connected to said at least one conductive pad on said second circuit board.

2. A semiconductor package according to claim 1, further comprising terminals electrically connected to said first electrical contact and said second electrical contact of said semiconductor die, said terminals being disposed on at least one of said substrates.

3. A semiconductor package according to claim 1, wherein each of said circuit board is an insulated metal substrate.

4. A semiconductor package according to claim 1, wherein said semiconductor die is a switching power semiconductor device which includes a control terminal, said control terminal being disposed on one of said first major surface of said die and said second major surface of said die and electrically connected to a conductive pad on one of said circuit boards, and electrically connected to a terminal disposed on one of said circuit boards.

5. A semiconductor package according to claim 1, wherein said semiconductor die is one of a MOSFET and an IGBT.

7. A semiconductor package according to claim1, wherein said conductive adhesive is either one of solder and conductive epoxy.

8. A semiconductor package according to claim 1, further comprising an epoxy underfilling disposed between said circuit boards.

9. A semiconductor package according to claim 1, further comprising a heatsink disposed on one of said circuit boards.

10. A semiconductor package according to claim 1, further comprising at least one heatsink disposed on each of said circuit boards.

11. A semiconductor package comprising:

a first thermally conductive substrate including a plurality of conductive pads disposed on a first major surface thereof;

a second thermally conductive substrate including a plurality of conductive pads disposed on a first major surface thereof;

a plurality of power semiconductor devices each including a first power contact on a first major surface thereof, a second power contact and a control contact on a second opposing major surface thereof;

a first layer of conductive adhesive interposed between, and mechanically connected to, a first power contact of each power semiconductor device and a respective conductive pad on said first thermally conductive substrate,

a second layer of conductive adhesive interposed between, and mechanically connected to, a second power contact of each power semiconductor device and a respective conductive pad on said second thermally conductive substrate;

and a third layer of conductive adhesive interposed between, and mechanically connected to, a control contact of each power semiconductor device and a respective conductive pad on said second thermally conductive substrate;

whereby each one of said contacts of said power semiconductor devices is electrically connected to a respective one of said plurality of conductive pads, and wherein said conductive pads on said thermally conductive substrate are interconnected to form part of a circuit.

12. A semiconductor package according to claim 11, further comprising output terminals connected to said power semiconductor devices through said conductive pads and disposed on at least one of said substrates.

13. A semiconductor package according to claim 11, wherein said thermally conductive substrate are insulated metal substrates.

14. A semiconductor package according to claim 11, wherein said power semiconductor devices are one of power MOSFETs and IGBTs.

16. A semiconductor package according to claim 11, wherein said conductive adhesive is one of solder and conductive epoxy.

17. A semiconductor package according to claim 11, wherein said power semiconductor devices are connected in a half-bridge configuration.

18. A semiconductor package according to claim 11, wherein said power semiconductor device are connected to form a plurality of half-bridge configurations.

19. A semiconductor package according to claim 11, further comprising a control device for controlling the operation of said power semiconductor devices.

20. A semiconductor package according to claim 11, further comprising epoxy filling spaces between said first and second thermally conductive substrates.

21. A semiconductor package according to claim 11, further comprising at least one heatsink in thermal contact with one of said thermally conductive substrates.

22. A semiconductor package according to claim 11, further comprising a heatsink in thermal contact with each one of said conductive substrates.

23. A method for manufacturing a semiconductor package comprising:

providing a first circuit board having at least one conductive pad disposed on a first major surface thereof;

printing a paste of a conductive adhesive on said conductive pad;

placing a semiconductor device on said conductive adhesive;

providing a second circuit board having at least one conductive pad disposed on a first major surface thereof;

printing a paste of a conductive adhesive on said conductive pad on said second circuit board;

placing said second circuit board over said semiconductor device such that said conductive adhesive on said second circuit board is in contact with said semiconductor device; and

applying heat to reflow said conductive adhesive.

24. A method according to claim 23, wherein said conductive adhesive is one of solder and conductive epoxy.

25. A method according to claim 23, further comprising filling spaces between said circuit boards with epoxy.

26. A method according to claim 23, wherein said circuit boards are insulated metal substrates.

27. A method according to claim 23, wherein each placing step is carried out by a pick-and-place method.